reconsideration is requested.

Rickard generally describes a bus acquisition system. However, rather than "a timer counter measuring **a time** during which **a signal** transmitted through said communication bus **continues to be a first logical level**," emphasis added, as recited in independent claim 1 of the present invention, Rickard describes a control unit 22 comparing contents of a current bus master priority register 24 with contents of a device priority register 26. See column 4, lines 3-7. In Rickard while the bus is used for data transfer, upon receiving a request from another device to use the bus, if the current data transfer is to end within a predetermined constant period, the data transfer is continued.

Furthermore, Rickard is silent as to teaching or suggesting, "a comparator **comparing the time** measured **with a threshold value** and outputting **an abnormality detection signal** indicating an abnormality in said communication bus **when the time surpasses said threshold value**," emphasis added, as recited in independent claim 1. Rather, in Rickard if a requesting device 18 has a higher priority than the current bus master, a requesting bus interface unit 16 asserts a bus request on line 37. See column 4, lines 7-9. Upon detecting the bus request, the current bus master **will continue to transmit messages** to its selected servant unit if the transfer of the messages can be completed in a predetermined amount of time. Emphasis added. See column 4, lines 9-13. Otherwise, the bus master must suspend the transmission of the messages and relinquish control to the bus unit, which asserted the bus request. See column 4, lines 13-16.

In other words, when another device requests the use of the communication bus, the order of priority in using the communication bus is compared rather than "comparing the time measured with a threshold value and outputting an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value," as recited in independent claim 1. Rickard fails to teach or suggest the claimed features of the timer and the comparator of the presently claimed invention. Because anticipation requires that each and every element of the claimed invention be disclosed in the prior art, it is the Applicants' position that Rickard fails to teach or suggest all the claimed features of independent claim 1. It is respectfully requested that independent claim 1 and related dependent claims 2-4 be allowed.

Referring to independent claim 5, this claim recites, "at least two timer counters each

measuring **a time** during which **a signal** transmitted through said communication bus **continues to be a first logical level**." Emphasis added. The arguments presented above supporting the patentability of this claimed feature are incorporated herein.

In Rickard rather than a register 24 "**cumulatively adding the time measured by at least one of said at least two timer counters**," emphasis added, as recited in independent claim 5, a bus unit 12 having a highest priority will be selected as the next bus master and its priority is stored in register 24. See column 3, lines 23-26 of Rickard. Furthermore, Rickard fails to teach or suggest that the "register being initialized at predetermined intervals," as recited in independent claim 5. In addition, independent claim 5 recites "a comparator comparing the time cumulatively added by said register with a threshold value and outputting an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value." The arguments presented above supporting the patentability of claim 1 having a similar claimed feature are incorporated herein to support the patentability of independent claim 5. It is the Applicants' position that Rickard fails to teach or suggest all the claimed features of independent claim 5. It is respectfully requested that independent claim 5 and related dependent claim 6 be allowed.

Independent claim 7 recites, "microcomputer connected to a communication bus, the microcomputer comprising: a timer counter measuring a time during which a signal transmitted through said communication bus continues to be a first logical level; and a comparator comparing the time measured with a threshold value and outputting an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value." The arguments presented above supporting the patentability of claim 1 are incorporated herein to support the patentability of independent claim 7. It is the Applicants' position that Rickard fails to teach or suggest all the claimed features of independent claim 7. It is respectfully requested that independent claim 7 be allowed.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: May 27, 2003

By: Alicia Choi
Alicia M. Choi
Registration No. 46,621

700 Eleventh Street, NW, Suite 500
Washington, D.C. 20001
(202) 434-1500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND claims 1, 5, and 7. The remaining claims are reprinted, as a convenience to the Examiner, as they presently stand before the U.S. Patent and Trademark Office.

1. (ONCE AMENDED) An abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

a timer counter [connected to said communication bus so as to measure] measuring a time during which a signal [having a first logical level is] transmitted [in] through said communication bus continues to be a first logical level; and

a comparator comparing the time measured by said timer counter with a threshold value and outputting an abnormality detection signal indicating an abnormality in said communication bus when the time [measured by said timer counter] surpasses [a] said threshold value.

2. (UNAMENDED) The abnormality detection device as claimed in claim 1, wherein said timer counter is initialized at intervals determined according to an event signal supplied thereto.

3. (UNAMENDED) The abnormality detection device as claimed in claim 2, comprising at least two units of said timer counter and said comparator, the timer counter in each of said units being individually initialized at said intervals.

4. (UNAMENDED) The abnormality detection device as claimed in claim 1, further comprising:

a plurality of comparison value registers respectively storing a plurality of threshold values; and

a selector selecting a threshold value from among said plurality of said threshold values according to a selection signal supplied thereto so as to supply said threshold value to said comparator.

5. (ONCE AMENDED) An abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

at least two timer counters each [connected to said communication bus so as to measure] measuring a time during which a signal [having a first logical level is] transmitted [in] through said communication bus continues to be a first logical level;

a register cumulatively adding the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals; and

a comparator comparing the time cumulatively added by said register with a threshold value and outputting an abnormality detection signal indicating an abnormality in said communication bus when [a] the cumulative time obtained by said register surpasses [a] said threshold value.

6. (UNAMENDED) The abnormality detection device as claimed in claim 5,

wherein said register supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value.

7. (ONCE AMENDED) A microcomputer connected to a communication bus, the microcomputer comprising:

a timer counter [connected to said communication bus so as to measure] measuring a time during which a signal [having a first logical level is] transmitted [in] through said communication bus continues to be a first logical level; and

a comparator comparing the time measured by said timer counter with a threshold value and outputting an abnormality detection signal indicating an abnormality in said communication bus when the time [measured by said timer counter] surpasses [a] said threshold value.